IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,	§	**Case No. 2:14-cv-902-RSP (Lead)**
Plaintiff,	§	
v.	§	
SAMSUNG ELECTRONICS CO., LTD., ET AL.	§	
HUAWEI TECHNOLOGIES CO., LTD., ET AL.	§	**Case No. 2:14-cv-687-JRG-RSP (Consolidated)**
MOTOROLA MOBILITY LLC	§	**Case No. 2:14-cv-689-JRG-RSP (Consolidated)**
Defendants.	§	

DEFENDANTS' RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

The present set of consolidated cases is part of a second wave of cases where plaintiff, Parthenon Unified Memory Architecture LLC ("PUMA"), has asserted many of the same patents and claims against seven defendants across three sets of consolidated cases. The defendants in this consolidated case, Motorola Mobility LLC, Samsung Electronics, Co., Ltd, Samsung Electronics America, Inc., and Huawei Electronics Co. Ltd. (collectively "Defendants"), hereby submit their combined Responsive Claim Construction Brief. The Court has already conducted a first *Markman* Hearing in the lead case against co-defendants LG and HTC, which took place on June 5, 2015. Defendants' arguments herein build upon those made at the prior hearing, rather than rehash previously made arguments, and take into account the Court's Preliminary Constructions as a starting point.

II. RELEVANT LEGAL STANDARDS

The Court is well versed in the general principles of claim construction. The process of construing a claim term begins with the words of the claims themselves. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-14 (Fed. Cir. 2005) (en banc). However, the claims "must be read in view of the specification, of which they are a part." *Phillips*, 415 F.3d at 1315 (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (*en banc*), *aff'd*, 517 U.S. 370 (1996)). "It is well-settled that, in interpreting an asserted claim, the court should look first to the intrinsic evidence of record, i.e., the patent itself, including the claims, the specification and, if in evidence, the prosecution history. Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." *Liquid Dynamics Corp. v. Vaughan Co.*, 355 F.3d 1361, 1367 (Fed. Cir. 2004) (quoting *Vitronics Corp.*, 90 F.3d at 1582). Other relevant principles of claim construction are applicable to this case and are discussed below.

III. AGREED/WITHDRAWN CONSTRUCTIONS

The parties have agreed that the term "simultaneously accesses the bus" means "accesses the bus at the same time." The parties have agreed that the term "translate" means "convert." The parties have agreed that the term "algorithmically translate" means "convert using at least one mathematical operation." Defendants would agree that the term "display device" means "screen and its circuitry" and that the term "display adapter" means "an adapter that processes images for a display device," just as the parties in the prior HTC-LG Case did. *See* Ex. N, HTC-LG *Markman* Transcript at 4:20-24.

Defendants also have elected to withdraw the terms "direct memory access engine" / "direct memory access (DMA) engine" / "DMA engine" and "refresh logic," and therefore no longer request that the Court construe these terms.

IV. THE COURT SHOULD ADOPT THE DEFENDANTS' PROPOSED CLAIM CONSTRUCTIONS BECAUSE THEY ARE THE MOST CONSISTENT WITH THE INTRINSIC AND EXTRINSIC RECORDS[1]

A. "bus"

Defendants' Proposed Construction[2]	PUMA's Proposed Construction
"a signal line or set of associated signal lines to which a number of devices are directly	No construction necessary.

[1] PUMA's opening brief takes liberties with the facts when it states: "STMicro previously asserted the '789 Patent in a patent infringement suit against Motorola Inc. in the Eastern District of Texas, Sherman Division. As part of that case, on July 16, 2004, **Judge Davis entered a claim construction order construing the terms 'shared bus,' 'real time operation' and 'arbiter,'** which are all implicated in the current claim construction dispute. *See STMicroelectronics, N. V.* v. *Motorola Inc.*, 327 F. Supp. 2d 687 (E.D. Tex. 2004). PUMA's constructions for those terms adopt the **constructions previously applied by Judge Davis**, which are consistent with how the terms are used in the patent specifications and with how a person of ordinary skill in the art would interpret these common terms. In contrast, Defendants' constructions deviate from Judge Davis's claim construction order by incorporating extraneous concepts that are inconsistent with the intrinsic and extrinsic evidence." Pl. br. at 1-2 (emphasis added). Not until page 5 of its brief does PUMA concede that Judge Davis did not *actually* construe these terms, but instead merely adopted the parties' agreed constructions. The Federal Circuit has recognized that parties may advance more specific constructions in later cases using the same claim term. *See Telcordia Techs., Inc. v. Cisco Sys., Inc.*, 612 F.3d 1365, 1373-74 (Fed. Cir. 2010).

[2] Defendants have amended their proposed construction for this term from the construction submitted in the parties' Joint Claim Construction Statement (Dkt. No. 66), as PUMA has also done with respect to terms "memory bus," "arbiter" and "monolithically integrated into."

connected and over which information may be transferred by only one device at a time"	Alternatively, "a signal line or set of signal lines to which a number of device are coupled and over which information may be transferred"

As demonstrated by the argument at the HTC/LG *Markman* hearing, the Court's preliminary construction is incomplete because it does not provide proper guidance on one vital aspect of a "bus", i.e., where one bus ends and another begins. Ex. N, *Markman* Transcript at 23:25-24:3; 28:7-24. Such guidance is critical in this case because asserted claims specifically require the use of one, but no more than one, bus. For example, the claims of the '459 and '194 patents recite that the components accessing the memory do so through only one bus. *See, e.g.*, Ex. G, '459 patent at claim 1; Ex. O, '194 patent at claim 1. Other asserted claims require a shared bus between multiple components. *See, e.g.*, Ex. H, '789 patent at claim 1.

Applying the Court's preliminary construction to a complex circuit containing two or many more distinct buses with components between them, one of ordinary skill may improperly declare the entire circuit to be one bus. To address this shortcoming, the Defendants' proposed construction is the Court's preliminary construction in the HTC/LG case with two important limitations. First, the phrase "by only one device at a time" is now proposed as a defining characteristic of a bus that is both supported by the intrinsic record and what a person of ordinary skill would have understood back in 1996. This phrase assists in clarifying where one bus ends and another begins because, as is described below, if two devices may transmit at the same time on different signal lines, those lines cannot be part of a single "bus." Second, Defendants propose that the word "coupled" be replaced by "directly connected," which is consistent with both the intrinsic record and Federal Circuit precedent. Use of the broadly defined term "coupled" is proposed by PUMA to sweep in as many potentially infringing components as it can. But the intrinsic record does not support such a broad construction.

1. The "bus" construction should reflect that only one device can transfer information on a bus at a time

A fundamental characteristic of a bus that should be included in any proper construction of the term is that only one device may transfer information on a bus at a time. A bus is, at bottom, an associated set of wires. *See* Ex. A, Stone Decl. ¶¶ 36, 37. When a device transmits a signal on a bus wire, that signal is transmitted over the length of the wire. *Id.* ¶¶ 33-36. That means a bus can carry only one associated set of signals at any given time. *Id.* ¶ 37, A; Ex. B Stone Dep. Tr. 35:16-36:12. If two or more devices try to transmit signals on the bus at the same time, they will create "contention" that leads to garbled data or destruction of both signals. Ex. A, Stone Decl. ¶¶ 38, 39; Ex. B, Stone Dep. Tr. 35:16-36:12. To prevent bus contention, there must be a mechanism to ensure that only one device is allowed to transfer information on the bus at a time. Ex. A, Stone Decl. ¶ 39. This concept of "one device at a time" is also supported by the specification. See Ex. G, '459 patent at 12:49-13:36. Thus, as reflected in Defendants' proposed construction, a key characteristic that defines a "bus" is that only one device on the bus can transfer information on the bus at a time.

To the extent that is not true, the box has been drawn too broadly, and what is inside is not a single "bus." *See, e.g.*, Ex. H, '789 patent at Fig. 1c (shown below). Figure 1c, for example, contains two buses, a PCI bus and an ISA bus, but they are separated by an intervening component—a PCI bridge 192. PCI bridge 192 is necessary to separate the two buses in order to prevent the above problems from occurring. Because devices can transfer information on the PCI bus and the ISA bus at the same time, that arrangement cannot be a single "bus."

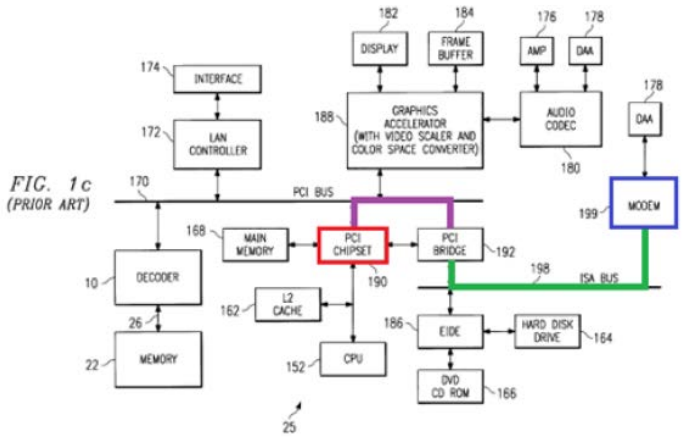
2. The use of the term "coupled" in PUMA's proposed construction makes it impossible to differentiate between one bus and two buses

Both PUMA's construction and the Court's preliminary construction in the HTC/LG case use the term "coupled" to describe the connection between the devices and the bus. As

extensively discussed at the HTC/LG *Markman* hearing, "coupled" is not precise enough to capture how devices are connected to a bus, particularly given PUMA's appeal in that case to construe "coupled" to include indirect connections.[3] Ex. N, *Markman* Transcript at 5:20-39:3. In fact, to construe "coupled" to include indirect connections would render the term "bus" meaningless, as all devices in the circuit would be "coupled directly or indirectly" to one another. *Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.*, 93 F.3d 1572, 1578 (Fed. Cir. 1996) (holding that broad claim interpretations that render a limitation "meaninglessly empty" are improper). Thus, the preliminary construction including "coupled" makes it impossible in this context to distinguish between the use of one bus and two buses for components to communicate with each other.

Figure 1c of the '789 patent again is illustrative of this phenomenon. As PUMA argued in its Reply Claim Construction brief in the earlier HTC-LG case, the components in Figure 1c, like the modem (item 199) "are coupled to the core logic chipset 190 through a bus 170." Dkt. No. 122 at 5. PUMA's color-coded figure from its Reply brief is reproduced below:

[3] Additionally, the word "coupled" cannot be presumed to have a known meaning in this family of patents, because the applicants declined to define it in response to a direct question from the Examiner. While prosecuting the '459 patent, the Examiner rejected claims under Section 112, first paragraph, stating: "it is not adequately clear what is meant by 'directly coupled' in this context (support for terminology in the specification? [What is the difference between 'coupled' and 'connected?' Between 'coupled,' 'directly coupled,' 'connected' and 'directly connected?']" *Id.* at PUMA0000779. The applicants declined to answer, instead completely removing both "coupled" and "directly coupled" from the claims in favor of "communicatively linked." *See generally* '459 patent claims.



Under its proposed construction, if the modem (blue) is "coupled to the core logic chipset 190 (red) through the bus 170 (purple), it must necessarily be connected to the bus 170 as well. But as PUMA rightly points out, in order to get to bus 170 the modem must communicate through a *separate* ISA bus 198 (green). So the modem must be "coupled" to the PCI bus (a first bus) using the separate ISA bus (a second bus). The modem accesses the PCI chipset therefore through two separate buses. But PUMA's use of "coupled" would allow the PCI and ISA buses to be viewed as one bus. Not only does the patent define them as two separate buses, it is technically infeasible for them to be a single bus because they operate under different specifications and signaling conditions that would prohibit such an arrangement. *Ethicon Endo-Surgery*, 93F.3d at 1578 (noting that it is entirely appropriate to look to the specification in construing claim terms). Yet that is precisely what the term "coupled" would allow if adopted. In short, PUMA's proposed construction should be rejected because it cannot distinguish a single bus from multiple buses, as even PUMA's own arguments demonstrate.

Adoption of the words "directly connected," as Defendants propose, would accomplish what the patentees intended and what a person of skill in the art at the time would understand without the risk of allowing this overly broad misinterpretation of the boundaries of a "bus." Turning to Fig. 1c again, the modem 199 is directly connected to the ISA bus 198, as is the EIDE

186 element. The modem is configured to communicate over the ISA bus 198, but cannot communicate over the PCI bus 170 without first going through a separate element—PCI bridge 192—that would convert the modem's communication protocol to match the PCI bus 170 protocol. Similarly, the PCI chipset 190 is directly connected to the PCI bus 170, just like the Graphics Accelerator 188. The decoder 10 is also directly connected to the PCI bus 170, but importantly it is not directly connected to the ISA bus 198. In order for the decoder 10, which is configured to communicate over the PCI bus 170 communication protocol, to communicate with the modem 199, it would need to match the protocol of the ISA bus 198, which is one of the functions of the PCI bridge 192. Ex. H, '789 patent, at 9:30-33. As can be seen, therefore, only devices that are "directly connected" to a bus may readily transfer information and communicate on that bus. Other devices that are not directly connected to a bus are not properly configured to communicate over that bus. Use of the words "directly connected" is thus more technically and legally precise and should be chosen over the more open-ended term "coupled," which suffers from all of the problems identified above and discussed at the prior Markman hearing.

Obfuscating the dispute over the "bus" construction and whether devices are "connected" to the bus are PUMA's misleading statements in its brief that prior art buses, such as the "Mbus," had intervening components like tri-state buffers and multiplexers. Pl. br. at 8. Contrary to PUMA's assertion, those components are not part of the bus itself. Rather, they are part of the bus interface circuitry that resides within the devices connected to the bus. *See* Ex. B, Stone Dep. Tr. at 36:25-37:6 and 49:15-50:5 (discussing tri-state buffering), 42:16-44:22, 47:17-22 (discussing multiplexed bus lines). Those components help the device operate properly when connected to the bus.

While this may seem like a slight distinction, it is important to properly distinguish a bus from the bus interface circuitry within each device because certain asserted claims in this case rely on this distinction. For example, claim 4 of the '045 patent recites "a video decoder configured to be coupled to the main memory via ***a first bus interface***," "a central processing circuit configured to be coupled to the main memory via ***a second bus interface***," and "an arbiter circuit coupled to…the ***second bus interface***…for controlling access to the bus via the respective ***bus interfaces*** of data to and from the first ***bus interface***[.]" Ex. Q, '045 patent, claim 4 (emphasis added).

The specification also makes the distinction between a bus and the bus interface circuitry of the devices using the bus. *See, e.g.*, Ex. G, '459 patent at 11:59-60 ("FIFO 30 is supplied with compressed data from bus 10 via an ***interface circuit PCI I/F 39***"); Figure 6 (item 39); 12:17-18 ("***bus interface 210*** for any system busses 170 to which it is coupled"); Figure 7 (item 210). Thus, even the patentees recognized that a bus is separate from the interface circuitry of the devices that intend to use the bus.

To summarize, a "bus," such as the Mbus, does not include the bus interface circuitry. Instead, the interface circuitry is located within the devices and separate from the bus. Thus, PUMA's supposition that an Mbus would not be considered a "bus" under Defendants' proposed construction is unfounded.

B. "memory bus"

Defendants' Proposed Construction	PUMA's Proposed Construction
"bus [as construed] that connects directly with a memory"	No construction necessary. Alternatively, "a signal line or set of signal lines to which a number of device are coupled and over which information may be transferred to a memory"

The term "memory bus" should be construed to mean a bus that connects directly with a memory. This construction is supported by the intrinsic record. For example, the asserted patents refer to the fact that "fast bus 70 is a memory bus." Ex. G, '459 patent at 8:13-14; Figure 2 (showing the memory bus connected directly to memory 50); 9:61-62; Figure 3 (showing memory bus 167 connected directly to main memory 168); 12:23-32; Figure 7 (showing memory bus 185 connected directly to frame buffer 184).

PUMA's proposed construction is overly broad because it contemplates that a bus could be a memory bus without having a memory directly attached to it.[4] PUMA's construction does not differ meaningfully from its construction of "bus" if data transmitted over the memory bus eventually makes its way to a memory, regardless of how many buses the data must travel over before it reaches the memory. The intrinsic record does not support that any bus in a data transmission path is a memory bus so long as the data eventually ends up at a memory. Rather, the intrinsic record supports a narrower construction—that a memory bus is a bus to which a memory is directly connected. *See*, *e.g.*, Ex. G, '459 patent at Figure 3 and 9:60-61 ("The main memory 168 is coupled to the memory interfaces 72 and 76 through a memory bus 167."); Figure 7 and 12:24-25 ("The frame buffer 184 is coupled to the memory interfaces 72 and 76 through a memory bus 185.").

C. "in real time"

Defendants' Proposed Construction	PUMA's Proposed Construction
Indefinite Alternatively, "fast enough to keep up with the input data stream wherein obtaining bus mastership does not consume bus cycles"	"fast enough to keep up with an input data stream"

[4] Indeed, PUMA's argument regarding the Mbus in that regard is both technically and legally incorrect. As discussed above, a person of skill in the art in 1996 would not have considered the intervening components or interfaces that PUMA refers to in its brief to be a part of the bus itself.

1. The asserted patents are intrinsically inconsistent as to the meaning of the term "real time"

The term "real time" is indefinite as used in the asserted patents because the applicants took inconsistent positions in the intrinsic record as to whether a PCI bus is a real time bus. And their inconsistent positions are based on inconsistent definitions of the term "real time." That inconsistency has introduced ambiguity such that the scope of "real time" cannot be determined with reasonable certainty in light of the specification and the prosecution history. *See Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014). When patents are intrinsically inconsistent as to the meaning of a claim term, that claim term is indefinite. *See, e.g.*, *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 723 F.3d 1363, 1369 (Fed. Cir. 2013), *vacated on other grounds and remanded*, 135 S. Ct. 831 (2015) ("Teva's attempt to resolve this ambiguity hinges in part on the prosecution history. But two of its prosecution statements directly contradict each other and render the ambiguity insoluble."). As more fully explained below, the patentees' inconsistent positions render the claims indefinite.

2. The asserted patents rely on bandwidth as the factor that determines real time performance

Several performance requirements affect whether a bus can operate in real time. Those include the bus bandwidth and the bus latency. Ex. E, Mangione-Smith Decl. ¶22; Ex. F, Mangione-Smith Dep. Tr. at 71:21-25, 91:4-15. The bus bandwidth refers to the amount of data that the bus can transfer at a given time. The bus latency refers to the delay for devices to get access to the bus to place data on the bus. These are separate concepts that have different impacts on a system. Bandwidth is the factor that the asserted patents rely on. The asserted patents neither focus on nor emphasize the importance of latency when they describe real time operation. Their focus is entirely on bandwidth.

For example, the claims focus on bandwidth. Claim 1 of the '789 patent recites "the bus having a ***sufficient bandwidth*** to enable the decoder to access the memory and operate in ***real time*** when the first device simultaneously accesses the bus." Ex. H, '789 patent at claim 1 (emphasis added). Claim 1 of the '315 patent similarly recites "the bus having ***sufficient bandwidth to transfer data in real time*** between the shared memory and the decoder." Ex. I, '315 patent at claim 1 (emphasis added). Finally, claim 1 of the '164 patent similarly recites "the memory bus configured to pass first data in real time" and "the memory bus configured to pass second data in real time[.]" Ex. J, '164 patent at claim 1.[5]

PUMA's own expert agrees that the asserted patents focus on bandwidth: "[t]he patents-in-suit clearly state that PCI is sufficient for [real time operation] because the key requirement for their application is bandwidth and PCI provides more than twice the amount of necessary bandwidth." Ex. E, Mangione-Smith Decl. ¶ 27. He also states that "[t]he patents-in-suit expressed a concern that bandwidth was the key bus performance factor that needed concern" and that the patents-in-suit were not concerned with latency. *Id.* ¶ 28. *See also* Ex. F, Mangione-Smith Dep. Tr. 56:13-20. Thus, according to PUMA's own expert witness, the asserted patents are only concerned with buses that have sufficient ***bandwidth*** to operate in real time.

The asserted patents confirm that a PCI bus had more than enough bandwidth for real time operation. *See* Ex. G, '459 patent at 5:14-20; Figure 4 (item 170). Dr. Mangione-Smith agrees that a PCI bus had enough bandwidth for real time operation. Ex. E, Mangione-Smith

[5] One patent in the '459 family even claims a PCI bus as a bus "having sufficient capacity to operate as the only bus in the computing system configured to transfer data in real time" in U.S. Patent 7,898,548, which is part of the family of the Asserted Patents sharing the same specification. *See* Ex. K, '548 patent at claims 1 and 7. Thus, there is no dispute that the patentees considered a PCI bus to be more than capable of delivering real time performance in their system.

Decl. ¶ 27 ("PCI provides more than twice the amount of necessary bandwidth"). Thus, it is not disputed that a PCI bus falls within the scope of the asserted claims because it had more than enough bandwidth to facilitate real time operation.

3. The prosecution history contradicts the specification and claims by stating that a PCI bus is not a real time bus because it has latency

Despite the fact that the patents clearly state that a PCI bus was a real time bus because it had enough bandwidth, the patentees told the Patent Office that a PCI bus used in the prior art was not a real time bus because it had latency.[6] *See* Ex. L, at PUMA0002591. That is the first time in the intrinsic record that latency was used to determine if a bus could operate in real time. The patentees distinguished the prior art Gulick patent[7] by asserting that the "PCI bus 120…is not a real time bus" because the PCI devices in Gulick "must obtain bus mastership, which consumes PCI cycles." *Id.* (emphasis in original). Consumption of PCI cycles is a direct reference to bus latency, but not bandwidth. Ex. A, Stone Decl. ¶ 26; Ex. E, Mangione-Smith Decl. ¶ 25. The patentees relied on this distinguishing point again in the next paragraph of their response to the Patent Office. There, they said that in Gulick, "the PCI devices must still obtain non-real-time bus mastership in order to receive data from main memory 11." *Id.* They went on to conclude that "[t]hus, Gulick's embodiment of FIG. 3 also falls short and fails to teach a memory bus configured to pass data in real time between a shared main memory and a decoder/encoder." *Id.* Importantly, the patentees did not comment on the bandwidth of Gulick's PCI bus or whether it was fast enough to keep up with an input data stream. Rather, they focused on latency, a separate consideration.

[6] Importantly, the relevant statement made by the patentees that a PCI bus is not a real time bus occurred almost 10 years after the term "real time" was construed in the earlier STMicroelectronics litigation involving the '789 patent.
[7] U.S. Patent No. 5,812,800.

The patentees' statements in the file history that a PCI bus is not a real time bus directly contradict the specification and claims. According to the specification, a PCI bus ***is*** a real time bus because it has enough bandwidth. But according to the file history, a PCI bus ***is not*** a real time bus because of its latency. That intrinsic conflict is irreconcilable and means the scope of the claims cannot be determined with reasonable certainty. Is the PCI bus a real time bus according to the patentees? Per the specification, yes it is. *See* Ex. G, '459 patent at 5:13-20. But per the file history, almost 10 years later, no it is not. *See* Ex. L, PUMA0002591. Patentees and PUMA cannot have it both ways – either the PCI bus is capable of real time operation or it is not. The public is entitled to rely on patentees' statements as an integral component to the notice function that the intrinsic record serves. *See, e.g., Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1347 (Fed. Cir. 1998) ("The public has a right to rely on such definitive statements made during prosecution. Notice is an important function of the patent prosecution process . . . ."); *Spectrum Int'l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1378 (Fed. Cir. 1998). Defendants contend that the patentees' contradictory statements render the term "real time" indefinite.

4. PUMA's "context" argument is based on a flawed legal premise

PUMA asserts that the above inconsistent statements about the PCI bus can be reconciled owing to contextual differences between the asserted patents and the prior art Gulick reference. *See* Dkt. No. 78 at 12; Ex. E, Mangione-Smith Decl. ¶¶ 24, 25. This "context" argument is based on a fundamentally flawed premise that the context of the prior art somehow limits its disclosure. As explained more fully below, prior art is relevant for all that it teaches, and PUMA's attempt to reconcile the contradictory intrinsic record is without support.

It is long-standing, black letter patent law that the context of use in the prior art does not limit the teachings of the prior art compared to the asserted claims. Indeed, the Federal Circuit

has repeatedly held that prior art is relevant for all that it teaches and is not limited by the specific problem that it was intended to solve. *See, e.g., In re Heck*, 699 F.2d 1331, 1331-33 (Fed. Cir. 1983) ("It makes no difference to this case that [the prior art] dealt with a different specific problem"); *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985) ("A reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect.").

Under the legal principles repeatedly articulated by the Federal Circuit in cases like *Heck* and *EWP*, PUMA's "context" argument must be rejected. The prior art Gulick patent is prior art for all that it teaches, regardless of its context. It is undisputed that Gulick taught a PCI bus, and that the patentees considered a PCI bus to have had sufficient bandwidth for real time operation in the asserted patents. Importantly, the patentees did not dispute that the prior art PCI bus had enough bandwidth for real time operation. Nor did they dispute that the prior art PCI bus was fast enough to keep up with an input data stream. Therefore, any supposed contextual differences between the asserted patents and the prior art do not change the fact the patentees made directly conflicting statements in the intrinsic record that render the term "real time" indefinite. A person having ordinary skill in the art could not read the intrinsic record and know whether a PCI bus falls within the scope of the claims. Ex. A, Stone Decl. ¶ 22.[8]

For these reasons, the asserted claims that recite "in real time" are indefinite under 35 U.S.C. § 112 ¶ 2 because of irreconcilable contradictions in the intrinsic record. *See Nautilus*, 134 S. Ct. at 2124.

[8] Because the patentees also introduced latency into their definition of real time without providing an objective measure for how much (if any) latency is acceptable, a person of ordinary skill in the art cannot know whether a bus with any latency (large or small) that otherwise meets the bandwidth requirements falls within the scope of the claims. *Id.* ¶ 27.

5. If the asserted claims reciting "in real time" are not indefinite, then the Court's construction must include the impact of latency which was part of the patentees' definition of "in real time"

As explained above, the asserted patents focus on bandwidth as determining whether a bus can operate in real time. It follows that a bus with sufficient bandwidth is fast enough to keep up with an input data stream. The construction "fast enough to keep up with an input data stream" therefore only refers to the bandwidth of the bus.

Yet, when faced with prior art having a bus with enough bandwidth, the applicants did not apply the "fast enough to keep up with an input data stream" definition proposed here. Rather, they modified their test for "real time" by introducing the concept of latency. Their use of latency to distinguish over prior art informs the meaning of the term "real time" as used in the asserted patents and the intrinsic record. That is because "[a]ny explanation, elaboration, or qualification presented by the inventor during patent examination is relevant, for the role of claim construction is to 'capture the scope of the actual invention' that is disclosed, described, and patented." *Fenner Investments, Ltd. v. Cellco P'ship*, 778 F.3d 1320, 1323 (Fed. Cir. 2015) (citation omitted). Moreover, the patentees' definition of "real time" from the file history must be applied to this case because "[c]laims may not be construed one way in order to obtain their allowance and in a different way against accused infringers." *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995).

PUMA's construction of the term "real time" fails to account for the definition used during prosecution and is therefore incomplete because the latency of a bus does not affect whether the bus is fast enough to keep up with an input data stream. In other words, even when used in a system with high latency, a bus with enough bandwidth is still capable of keeping up

with an input data stream. Yet, the latency can result in undesirable results that prohibit-real time operation—just as the patentees claimed when distinguishing the Gulick reference.[9]

The bus latency may not impact the bus's ability to keep up with the input data stream. It impacts the speed with which a new data stream can be placed on the bus in the first case. *See* Ex. B, Stone Dep. Tr. at 21:2-22:14. But even where there is a substantial delay (i.e., latency) for a new data stream to be placed on the bus, once it is placed on the bus, a bus with enough bandwidth is still fast enough to keep up with that input data stream. Because the patentees relied on latency to distinguish over the prior art instead of bandwidth, the construction of the term "real time" ***based on this intrinsic record*** must include that as well. Otherwise, the construction is ambiguous and disregards the patentees' own statements, in violation of the public notice function of the patent system.

For these reasons, PUMA should be held to the definition of "real time". On this intrinsic record, the term "real time," if not indefinite, must include the fact that no bus cycles are consumed while switching bus masters. That is the definition of "real time" used by the patentees. Accordingly, Defendants have proposed that the clause "wherein obtaining bus mastership does not consume bus cycles" be added to the construction proposed by PUMA. The definition used by the patentees to obtain the '164 patent should be part of the definition in this litigation.[10]

[9] Ex. B, Stone Dep. Tr. at 21:2-14 and 21:24-22:14.

[10] PUMA's expert Dr. Mangione-Smith also opined that the claims are not invalid as indefinite even with the statements about the prior art Gulick patent because Gulick was directed to a different context. Ex. E, Mangione-Smith Decl. ¶¶ 24, 25. Because Dr. Mangione-Smith has opined on this issue of invalidity, his rationale must also apply to the issues of infringement to be decided later in this case. As the Federal Circuit has repeatedly held, "[i]t is axiomatic that claims are construed the same way for both invalidity and infringement." *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003). Thus, whatever contextual differences exist between the asserted patents and Gulick must also be applied to determining the issue of infringement later on.

D. "arbiter" / "arbitration circuit" / "memory arbiter" / "arbiter circuit"

Defendants' Proposed Construction	PUMA's Proposed Construction
"circuitry that provides direct access without multiplexing inputs"	"circuitry that uses a priority scheme to determine which requesting device will gain access"

The crux of the parties' dispute is whether the claims cover i) *any* type of arbiter (PUMA's contention) or ii) the allegedly inventive arbiter distinguished by the inventors from prior art arbiters (Defendants' contention). PUMA (1) ignores the applicants' clear statements during prosecution, (2) ignores the fact that the applicants did not rescind their disclaimer at any time during the prosecution of the '459 patent or any related patent, and (3) ignores clear Federal Circuit precedent that the disclaimer in the '459 patent applies to all related patents. Defendants' construction largely mirrors PUMA's, but reflects the applicants' disclaimer during prosecution of one specific prior art method for arbitration.

The Examiner rejected the pending claims of the '459 patent, which recited an arbiter that provided various devices "access" to a memory (e.g., Ex. D at PUMA0000611, claim 37), over U.S. Patent No. 5,809,538 to Pollmann et al. *Id.* at PUMA0000686-687. Pollmann disclosed the following architecture, in which the arbiter was positioned between the memory and the device that needed to access the memory:

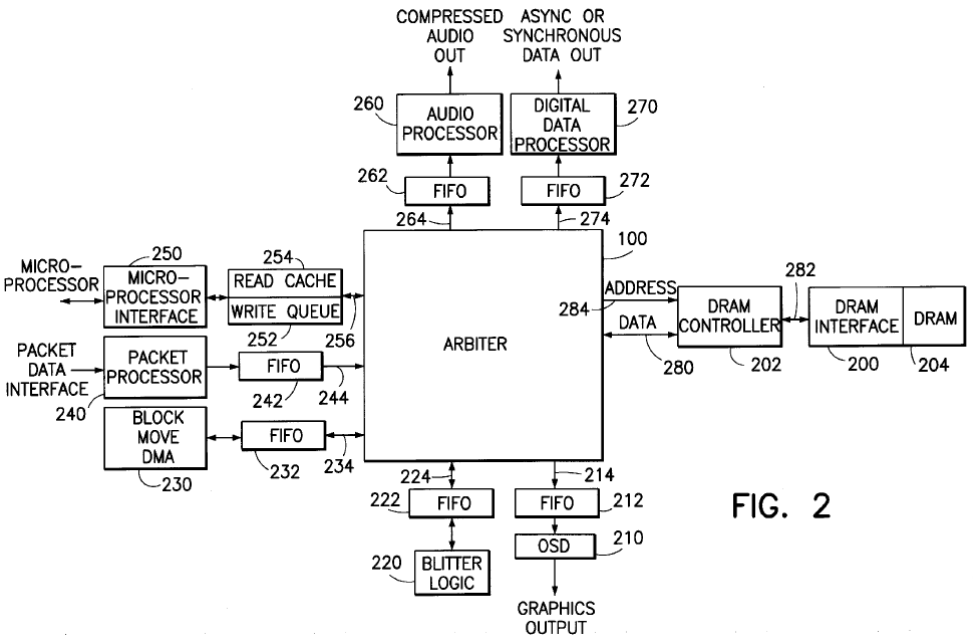


FIG. 2

Ex. D at Fig. 2. In response, the applicants amended the claims to recite "direct access" (e.g., *id.* at PUMA0000757, claim 18) and stated that their arbiter provided "direct access" rather than "multiplex[ing]" devices to a memory. *Id.* at PUMA0000763-64. This argument, which applicants made to attempt to gain allowance of the claims, is the basis of the difference between PUMA's and Defendants' constructions: that the arbiter must provide direct access. *Fenner Investments, Ltd. v. Cellco P'ship*, 778 F.3d 1320, 1323 (Fed. Cir. 2015) ("[T]he interested public has the right to rely on the inventor's statements made during prosecution, without attempting to decipher whether the examiner relied on them, or how much weight they were given.").

PUMA argues that "the patentees did not redefine the term 'arbiter' but rather added other surrounding language to traverse the cited art." The applicants certainly amended the claims. But they did so in concert with an argument to the Patent Office that explained how the claimed arbiter was different than the prior art arbiter. That argument resulted in a disavowal of scope regarding a method of arbitration—not specific claim language—and that scope is

properly excluded from all claims that would cover that method of arbitration. *See, e.g., Hakim v. Cannon Avent Group, PLC*, 479 F.3d 1313, 1316-18 (Fed. Cir. 2007) (construing claims that recited an "opening" to be limited to a "slit" based on the applicant's argument that the slit distinguished its invention from the prior art).

PUMA next points out with great fanfare that the claims discussed above were subsequently canceled and rewritten, inferring that should eliminate any possibility of a disclaimer. That is not the law. *See, e.g., Hakim*, 479 F.3d at 1317 ("Although a disclaimer made during prosecution can be rescinded, permitting recapture of the disclaimed scope, the prosecution history must be sufficiently clear to inform the examiner that the previous disclaimer, and the prior art that it was made to avoid, may need to be re-visited.").

Yes, PUMA ignores the fact that in further prosecution the applicants made no suggestion that they wished to rescind the disclaimer and have the Examiner reconsider Pollmann against those rewritten, broader claims. Instead, the patentees instead re-affirmed that their arbiter was decoupled from bus access, thereby permitting direct access, just as they had argued during prosecution of the '459 patent family. *See* Ex. C, PUMA0001247-1259 at 1256; Ex. C, PUMA0001276-1295 at PUMA0001283. PUMA cannot have the disclaimed scope back now. *Hakim*, 479 F.3d at 1317.

Finally, PUMA suggests it would be "problematic" for this disclaimer to apply to the other patents related to the '459, but again offers no case law in support—likely because the law is exactly the opposite. *See, e.g., Droplets, Inc. v. eBay, Inc., 2014 WL 4217376*, * (E.D. Tex. 2014) (Payne, J.) ("This disclaimer finding applies to all of the patents-in-suit.") (citing *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1306-1307 (Fed. Cir. 2007) ("We have held that a statement made by the patentee during [the] prosecution history of a patent in the

same family as the patent-in-suit can operate as a disclaimer.").). This is all the more so when the patents at issue share a common specification[11] and use the same disputed term. *See, e.g., Microsoft Corp. v. Multi–Tech Sys., Inc.*, 357 F.3d 1340, 1350 (Fed. Cir. 2004) (applying a disclaimer to such a family of patents, both patents prosecuted after the disclaimer and a patent that had already issued when the disclaimer was made). It is further confirmed by the fact that the patentees relied on these structural features multiple times in prosecution. The patentees themselves have also acknowledged the substantial overlap in the inventions of these patents and the fact that they incorporate each other by reference. Dkt. No. 78 at 1. Thus, these terms should be construed consistently across all patents in which they appear.

E. "control circuit"

Defendants' Proposed Construction	PUMA's Proposed Construction
"an electronic control device that is separate from the CPU or processor"	No construction necessary

This dispute boils down to whether the "control circuit" is an *electronic device* that is *separate from* the CPU/processor. In describing "the present invention," the patentee confirmed both characteristics:

> Broadly stated, *the present invention embodies a control circuit* for use in a computer system. The computer system is controlled by an operating system and has a main memory. *An electronic device is coupled to the processor* and the main memory *and is configured to request* continuous use of several portions of the main memory *from the operating system*.

Ex. P, '464 patent at 3:37-43 (emphasis added). This passage sums up the uniform disclosure of the '464 patent specification.

The drawings tell the same story. Element 114 in Figure 1 is "an MPEG 2 decoder under the present invention," an expanded view of which is shown in Figure 2:

[11] The '789 and '459 patents incorporate each other's specifications by reference, and the rest of the patents are continuations of the '459 patent.

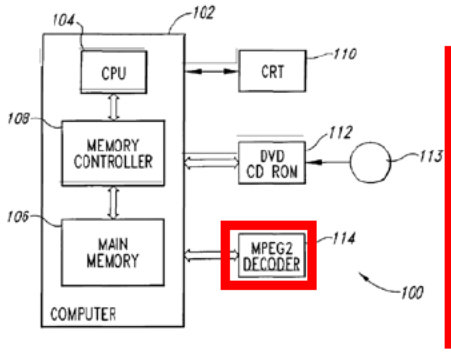


Fig. 1

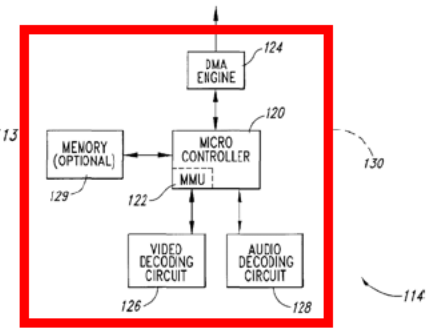


Fig. 2

The '464 patent uniformly discloses microcontroller 120 inside MPEG decoder 114 as the entity that requests memory from the operating system and translates between noncontiguous and contiguous addresses—the tasks of the claimed "control circuit." *See, e.g.*, Ex. P, '464 patent at 6:63-7:50. Figures 1 and 2 confirm that the entirety of MPEG decoder 114, including microcontroller 120, is not part of CPU 104, the operating system, or even computer 102—instead, the MPEG decoder is a separate device coupled to computer 102 just like CRT (display) 110 and DVD/CD ROM player 112.

The patentee repeatedly and consistently characterized this architecture as "the present invention." *See, e.g.*, Ex. P, '464 patent at 1:19-20 ("The present invention relates to the field of *electronic systems* requiring blocks of memory"); 6:60-62 ("the present invention *shares* the main memory 108 *with the computer 102*"); 9:14-21 ("The present invention *interacts with the Windows 95 operating system* 152 to *act like* a software application" but "*actually employs hardware*" that "*is not a CPU, or other processor*, or Intel-based microprocessor") (all emphasis added).

Applicants repeated their consistent message during prosecution, specifically arguing the separateness of the "control circuit" to the Patent Office in order to gain allowance. In response to a rejection, Applicants amended independent claim 25 to include the "control circuit" and argued that "Herrell et al. does not teach the administration of a memory management method

through a *separate control circuit* . . .” Ex. M at PUMA0000506-7 (emphasis added).

Given these repeated and consistent representations, heeding PUMA’s call not to construe this term would improperly award it the claim scope surrendered in the patent and during prosecution. *See, e.g., Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007). In *Verizon*, the parties disputed whether a claimed “localized wireless gateway system” was required to “compress[]/decompress[] and packetiz[e] voice signals.” *Id.* The Federal Circuit held that the district court had erred by not including these features in its construction, finding that the “Disclosure of the Invention” section of the patent described the disputed features in the context of “the present invention” and concluding that “[w]hen a patent thus describes the features of the ‘present invention’ as a whole, this description limits the scope of the invention.”). *Id.* As shown above, that is precisely the situation here.

PUMA’s arguments neither address nor affect the above calculus. First, PUMA argues that construing “circuit” as “device” is “unhelpful.” Pl. br. at 21. To the contrary, not only is “device” the very word the patent uses to describe the claimed “control circuit” (3:40-43), such a construction unquestionably grounds the “control circuit” in the realm of physical hardware, not merely a piece of software running on the CPU and under the operating system. Again, “[t]he present invention relates to the field of *electronic systems* requiring blocks of memory.” ’464 patent at 1:19-20 (emphasis added). Making that distinction clear will be very helpful to the jury.

Second, PUMA argues that the jury would be confused because the patent does not explain what it means for two things to be “separate.” Pl. br. at 21. PUMA’s point is unclear. As shown above, the patentee used the word “separate” to distinguish prior art and thus limited the claims accordingly. The fact that the patent does not provide a special definition for

"separate" simply reinforces the fact that the jury should be well-equipped to understand the word based on common parlance—just as the Examiner presumably did.[12]

Finally, PUMA alleges that the surrounding claim language adequately defines "control circuit," but the examples it provides appear on their face to reinforce Defendants' proposed construction (e.g., "the 'control circuit' is coupled . . . to the processor" and "configured to 'request . . . from the operating system.'"). In other words, there should not be a dispute. Defendants therefore respectfully request that the Court adopt Defendants' clarifying construction rather than leaving the parties to argue the scope of "control circuit" to the jury. *O2 Micro Intern v. Beyond Innovation Technology*, 521 F.3d 1351 at 1362-63 (Fed. Cir. 2008).

F. "directly supplied" / "directly supplies"

Defendants' Proposed Construction	PUMA's Proposed Construction
Plain and ordinary meaning. Alternatively, "supplie[d/s] without intervening components"	"supplie[d/s] without being stored in main memory for purposes of decoding subsequent images"

Given that both proposed constructions for "directly supplie[d/s]" incorporate the word "supplie[d/s]," the dispute has essentially been reduced to what "directly" means – e.g., whether it means "without intervening components" as Defendants propose or "without being stored in main memory for purposes of decoding subsequent images" as PUMA argues.

PUMA's proposal injects two flawed limitations: "without being stored in main memory," which seeks to read an embodiment into the claims, and "for purposes of decoding subsequent images," which is redundant given the language of the affected claims.

[12] The fact that the patent discloses an embodiment where the control circuit and processor are disposed on a single chip is irrelevant to this question of whether the control circuit and processor are separate functional entities. The latter is a question of architecture; the former merely of packaging.

To support the limitation "without being stored in main memory," PUMA cites to just one single statement in the specification:

> "a buffer associated with bidirectional images is not required, these bidirectional images B being directly supplied to display adapter 120 as they are being decoded." *See* Op. Br. at 18 (*citing* '194 Patent at 10:39-42).

But the very same section of the patent clarifies that this is just "another embodiment" (*id.* at 10:22), unlike other disputed terms such as "control circuit" where the patent recited "the present invention," and the "onboard memory" terms where the patent recited "according to the invention." Nor did the patentees disclaim any scope of "directly supplied" in the specification or file history, as they did with respect to "bus," "real time," and the "arbiter" terms. Here, they simply described "another embodiment"—an example.

And PUMA cannot pass off this example as a definition of "directly supplied." First, a plain reading of the statement simply indicates that when images B are directly supplied to display adapter 120 as they are being decoded, a buffer associated with these images is not required. Importantly, it does not say that *if* the B images are not stored in a buffer, then they *are* directly supplied.

Second, this understanding of the statement cited by the Plaintiff is confirmed simply by looking at Figure 4 of the same '194 patent, in reference to which the statement was made:

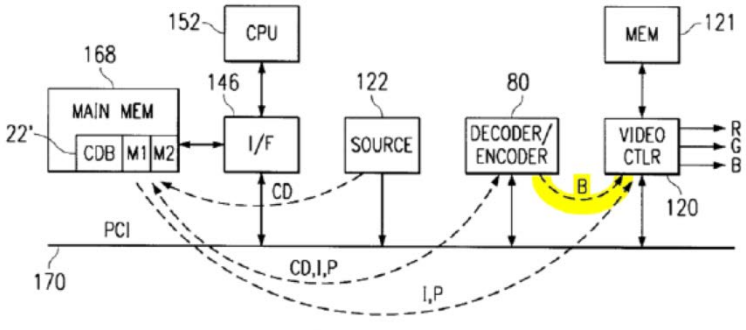


FIG. 4

While it is true that B images are not supplied to a buffer memory on their path from the decoder to the display adapter, neither are they supplied to any other component, such as the I/F 146 or CPU 152. But under PUMA's narrow construction, an image supplied by the decoder to other components such as the I/F 146, or CPU 152, or any memory other than the "main memory," for that matter, before being supplied to the display adapter would still be considered "directly supplied" by the decoder to the display adapter. This is completely at odds with the plain and ordinary meaning of "directly," and clearly Plaintiff's one citation describing "another embodiment" is insufficient to redefine it.

Plaintiff's second limitation, "for purposes of decoding subsequent images," is flawed as well because it is redundant given the surrounding language of the claims that include the "directly supplie[d/s]" language. To illustrate, several affected claims already specify that the image being supplied is "an image under decoding which is not used to decode a subsequent image." *See, e.g.*, Ex. R, '368 Patent Claims 2, 14, and 21; '753 Patent Claim 3. The limitation "for purposes of decoding subsequent images" is therefore redundant because the image would necessarily not be stored for purposes of decoding subsequent images when the claim already states that the image is not used to decode a subsequent image.

Defendants' proposed construction, on the other hand, gets at the plain meaning of "directly" in the context of the asserted patents in suit: "without intervening components." In particular, it indicates that an image that, after decoding and before reaching the display adapter, is *supplied to any component, including the main memory,* is not "directly supplie[d/s]" by the decoder to the display adapter. This proposal is consistent with the entire intrinsic record.

G. "monolithically integrated into" / "integrated into"

Defendants' Proposed Construction	PUMA's Proposed Construction
"formed within"	"formed on a single semiconductor chip with"

The dispute here centers on whether the first component must be formed ***within*** the second component as Defendants propose, or merely ***with*** the second component and "on a single semiconductor chip" as PUMA argues.

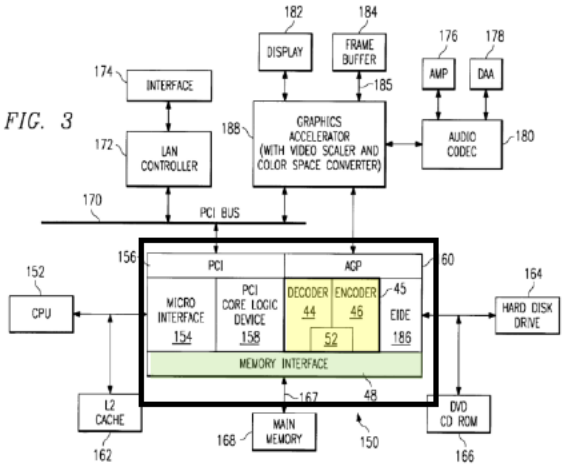
PUMA's proposal is flawed in two ways. First, PUMA's construction is inconsistent with the asserted patents' claims. To illustrate, the claims of the '164 patent explicitly differentiate between integrating components ***with*** the decoder/encoder, and integrating components ***into*** the decoder/encoder. On one hand, claim 8 narrows claim 1 by specifying that certain components "are **integrated *with*** the decoder/encoder." Claim 12, on the other hand, narrows claim 1 by specifying a different form of integration whereby certain components "are monolithically **integrated *into*** the decoder/encoder." *Karlin Tech. Inc. v. Surgical Dynamics, Inc.*, 177 F.3d 968, 972 (Fed. Cir. 1999) ("[D]ifferent words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope."). Given the explicit differentiation between integrating components ***with*** the decoder/encoder, and integrating components ***into*** the decoder/encoder, it would be improper to construe this term in a manner that obliterates this distinction, as Plaintiff does by proposing that "integrated ***into***" be construed as "formed … ***with***."

Second, PUMA's construction injects an entirely new element, "on a single semiconductor chip," into the claim language by relying strictly on extrinsic dictionary evidence without identifying any intrinsic evidence whatsoever in support. It is improper to import elements from extrinsic evidence where the four corners of the patent never disclose that element. *Markman v. Westview Instruments*, 52 F.3d 967, 981 (Fed. Cir. 1995) ("Extrinsic evidence is to be used for the court's understanding of the patent, not for the purpose of varying or contradicting the terms of the claims."). In this instance, the term "semiconductor chip"

appears neither in any claim nor the rest of the specification for that matter. Thus, it would be improper here to reach outside the asserted patents to limit this term to a "semiconductor chip," or even further to a formation "***on a single*** semiconductor chip."

Defendants' proposed construction, on the other hand, is supported by both the claim language and specifications. For example, Figure 3 of the '789 patent, below, depicts a block diagram of the claimed system. While this is arguably an embodiment, the specification equates Figure 3's placement of the decoder/encoder [45] and the memory interface [48] within the core logic chipset [150], with the integration of components 45 and 48 into component 150. (*See* Ex. H, '789 patent at 8:37-40 ("FIG. 3 shows a computer where the decoder/encoder 45 and the memory interface 48 are integrated into a core logic chipset 150."), 8:30-34 ("The decoder/encoder 45 is preferably monolithically integrated into the first device as shown in FIG. 3 and FIG. 4. In FIG. 3 the decoder/encoder 45 is integrated into a core logic chipset 150.").)

FIG. 3



H. "[first, second, third] onboard memor[y,ies]"

Defendants' Proposed Construction	PUMA's Proposed Construction
"[first, second, third] memory within the decoder"	No construction necessary

As the Court well understands by this juncture, the patents-in-suit are generally directed to devices sharing an external memory over a bus. The patents repeatedly distinguish the alleged invention from the use of dedicated memory on a device. See, e.g., Ex. G, '459 patent at 5:33-37. With that in mind, claim 1 of the '315 patent recites both a "shared memory" and an "image decoder circuit" that "includes" three "onboard memories." Defendants' construction simply makes clear that "onboard" means the memory must be part of the decoder, not simply accessible to it (as is the separately recited "shared memory").

Though the term "onboard memory" does not appear in the patents, they explicitly disclose a decoder that includes three First-In-First-Out ("FIFO") memories. *See* Ex. I, '315 patent at 11:57-12:2; Fig. 6 (FIFOs 30, 35, and 37):[13]

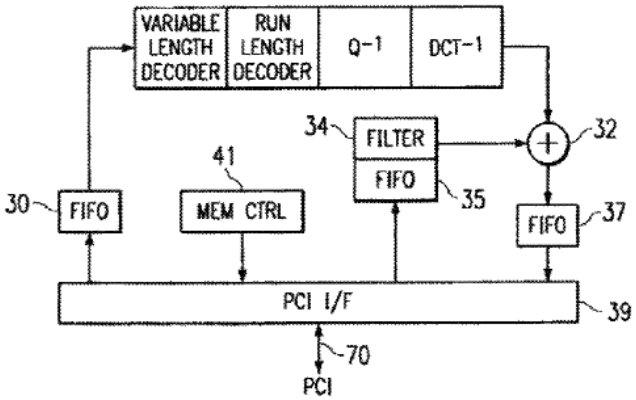


Fig. 6

The patent describes the above Fig. 6 as "an electrical diagram, in block form, of an embodiment of an MPEG decoder architecture according to the present invention." '315 patent at 6:22-24. That architecture shows the three memories are within the decoder circuit, or

[13] Dependent claim 7 further confirms that these three FIFOs are synonymous with the recited "onboard memories," perfectly tracking Fig. 6 and the corresponding disclosure. Ex. I, '315 patent at 16:24-29 "wherein the first onboard memory is configured to supply data to a variable length decoder, the second onboard memory is configured to store macro blocks from a previously decoded image, and the third onboard memory is configured to store image data from the adder.

"onboard" the decoder. PUMA offers no support for its fanciful argument that the term somehow relates to being located on the same circuit board as the decoder. The claims do not recite circuit boards at all, and the single reference to "motherboard" and "removable boards" PUMA identifies ('315 patent at 2:66-67) is discussing the prior art and does not relate to (much less contradict the above explicit disclosure of) where a decoder's "onboard" memory resides.

I. "contiguous" / "non-contiguous"

Defendants' Proposed Construction	PUMA's Proposed Construction
"contiguous": "adjacent" "non-contiguous": "non-adjacent"	No construction necessary

"Contiguous" and "non-contiguous" are not words the jury is likely to understand, particularly in the context of computer memory addresses—at bottom, numbered storage locations. The essence of the alleged invention of the '464 patent is to translate "non-contiguous" addresses into "contiguous" addresses so that various blocks of memory with gaps in between will appear to be a single, large block of memory. Thus, for example, a contiguous set of memory addresses from address 105 to address 109 would include addresses 105, 106, 107, 108, and 109. *See generally* Defendants' Technology Tutorial at slides 52-55 (showing a "contiguous" block of memory including addresses 1, 2, 3, and 4); PUMA's Technology Tutorial at 6:30-7:56 (same).

Defendants' concern is that the jury, to the extent it has heard the terms "contiguous" and "non-contiguous," may be familiar with them in other contexts. A lay person might, for example, think of the 48 "contiguous" United States in which most states share borders with multiple other states, and might be confused about how the terms apply to computer addresses. Defendants believe that the terms "adjacent" and "non-adjacent" will allow the jury to more

readily understand that each memory address in a contiguous block must immediately follow the prior address and be immediately followed by the next address.

PUMA takes potshots at Defendants' construction through an inapt analogy to a series of buildings. PUMA's analogy conflates ***addresses*** with ***physical locations***.[14] The claims are clear on their face that what must be contiguous or non-contiguous are the memory addresses, not the physical gates on the semiconductor die in which units of memory are stored. Compounding its error, PUMA argues that these terms would be well understood by one of skill in the art, but takes no position on what that understanding would be.[15] This stands the inquiry on its head: the point of claim construction is not to leave an expert to later argue claim scope to the jury, but to assign "a fixed, unambiguous, legally operative meaning to the claim." *Liquid Dynamics*, 355 F.3d at 1367. Defendants respectfully request that the Court do so here.

V. CONCLUSION

Defendants respectfully request that the Court adopt their proposed claim constructions and find that the term "real time" is indefinite as used in the asserted claims.

Dated: July 2, 2015

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[14] Another serious flaw in PUMA's building analogy is that unlike memory locations, many property addresses do not immediately follow each other in sequence. For example, a block of buildings might have addresses numbered 501, 508, 519, 521, 521 ½, 522, 535, and 540. If PUMA would consider such a block of addresses to be "contiguous," that would appear to eliminate any meaningful difference between "contiguous" and "non-contiguous." If, on the other hand, PUMA agrees that a contiguous block of memory locations represents an unbroken sequence (e.g., 501, 502, 503, 504, 505, 506, etc.), then there should be no dispute.

[15] Compare this silence with other disputed claim terms for which PUMA does explicitly state what it believes the understanding of one of skill in the art would be. *See, e.g.*, Pl. br. at 25 ("onboard memory").

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CERTIFICATE OF SERVICE

I hereby certify that on July 2, 2015, I electronically filed the foregoing document with the clerk of the court for the U.S. District Court for the Eastern District of Texas, Marshall Division, using the electronic case filing system of the court in compliance with Local Rule CV-5(a). The electronic case filing system sent a "Notice of Electronic Filing" to the attorneys of record who have consented in writing to accept this Notice as service of this document by electronic means.

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